Amendments to the Specification

Please replace the paragraph that begins at page 13, line 13 with the following amended paragraph:

FIGS. 1-7 having been described above, attention is now directed to FIGS. 8-10B which show embodiments of [[a]] reference signal generators of the invention. In particular, the reference signal generator 200 of FIG. 8 includes the DCXO 20 of FIG. 7, the frequency controller 38 of FIG. 1, a buffer amplifier 202 and an amplitude controller 204.

Please replace the paragraph that begins at page 13, line 18 with the following amended paragraph:

Although the buffer amplifier 202 may be, for example, the output amplifier 206 of FIG. 7, it is more generally any buffer inserted between the DCXO and various system elements (210 in FIG. 7) that require the buffer's reference signal. These system elements typically include integrated circuits (e.g., an applications processor, a polyphonic ring tone generator and other circuits that conform to wireless network standards (e.g., Bluetooth and Wi-Fi)) that present [[a]] an input impedance which is primarily formed by their parasitic capacitances. This capacitive load will vary depending on the particular mix of circuits that require the reference signal.

Please replace the paragraph that begins at page 17, line 16 with the following amended paragraph:

Because the enable signal is not initially present, the circuits of the reference signal generator (200 in FIG. 8) are allowed to stabilize. When the enable signal is provided, the clock 294 is passed through the gate 288 to the gate 290. ~~The~~ Because of the presence of the window signal, the clock 294 passes through the gate 290 (the deglitch circuit will be subsequently described) and is counted in the counter 284 (e.g., with a series 294 of flip-flops). The counter's gain control signal alters so as to successively increase the combined resistance of the

charging resistors 226 in FIG. 10A which causes the reference amplitude of the reference signal to successively decrease.

Please replace the paragraph that begins at page 17, line 25 with the following amended paragraph:

When it decreases below that amplitude determined by the first and second threshold selectors (246 and 247 in FIG. 10A), the pulse trains at the ALC output port (260 in FIG. 10A) cease. This output port is the same as the input port 260 in the ALC logic 280 of FIG. 10B. Accordingly, the pulse trains at this port cease which turns off the gate 290 so that the gate 290 blocks the clock 294 and stops the counter 284. The reference amplitude of the reference signal has now been automatically reduced to the amplitude determined by the selected tap transistors 253 in the first and second threshold selectors 246 and 247 of FIG. 10A.

Please replace the paragraph that begins at page 18, line 19 with the following amended paragraph:

When the first and second pulse trains initially cease, the disable signal has not yet closed the gate 288. If a spurious signal were to be generated and coupled to the input port 260 of the ALC logic 280, it might permit the clock signal 294 to pass through the gate 290 and trigger the counter and the reference amplitude of the reference signal would be decreased below the intended level. This might endanger the integrity of the systems that receive the reference signal.